

SEMICONDUCTOR DEVICE

5 BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to an area-array semiconductor device having arranged external electrode terminals on the bottom surface of a chip or the bottom
10 surface of a package, and more in detail to the semiconductor device having a reduced size of the chip or the package and to increase the number of the external electrode terminals.

(b) Description of the Related Art

15 With the higher integration of a semiconductor device, the number of external electrode terminals for externally and electrically connecting a chip or a package mounting the chip is increased. On the other hand, the miniaturization of the chip or the package is advanced to
20 reduce the size of the pitch between the terminals of internal electrode terminals. Accordingly, the pitch of the interconnect pads formed on a packaging substrate or a mounting board for packaging the chip thereon is also reduced, and the reduced pitch makes it difficult to
25 arrange the interconnects on the packaging substrate or

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mounting board. As a result, the miniaturization of the chip and the package is hardly realized.

A semiconductor device 101 as shown in Fig.1 is an example of forming internal electrode terminals on the bottom surface of a chip 103 which is mounted on a packaging substrate 102. A plenty of ball electrodes 131 acting as external electrode terminals are arranged on the bottom surface of the chip 103 in a BGA (ball grid array) arrangement. The packaging substrate 102 includes, on the top surface thereof, interconnect pads 121 corresponding to the ball electrodes 131 of the chip 103 and interconnect lines 122 for connecting the respective interconnect pads 121. On the bottom surface of the packaging substrate 102 are arranged packaging ball electrodes 124 connected to the interconnect pads 121 and the interconnect lines 122 through intermediary of via-plugs 123. The chip 103 is mounted over the packaging substrate 102 and covered and sealed with resin 105, and the ball electrodes 131 of the chip 103 are connected to the interconnect pads 121 by soldering. The semiconductor device 101 is mounted on a substrate 104, and the packaging ball electrodes 124 are connected to interconnects pads 141 formed on the top surface of the substrate 104.

The interconnect pads 121 arranged on the

packaging substrate 102 surface as shown in Fig.2 are substantially identical with the ball electrodes 131 formed on the bottom surface of the chip 103 with respect to their arrangements. The conventional interconnect pad arrangement has so-called peripherals including a signal line terminal (S-terminal), a power source terminal (V-terminal) and a ground terminal (G-terminal) arranged on a single line and disposed in a region corresponding to the outer peripheral of the chip 103. As shown in Fig.2, the respective interconnect pads 121 including the S-terminal, the V-terminal and the G-terminal are arranged in the shape of a lattice by keeping specified intervals. Each of interconnect lines 122 is connected to each of the interconnect pads 121, and extends toward the outer region of the chip. The interconnect lines 122 connected to the interconnect pads 121 existing in the inner part outwardly extend between the interconnect pads 121 existing in the outer part, and the front end of the interconnect line 122 is electrically connected to the packaging ball electrodes 124 on the bottom surface of the packaging substrate 102 through intermediary of the viaplugs 123 as shown in Fig.1.

However, in the arrangement of the above interconnect pads, due to the density of the interconnect pads 121 and the interconnect lines 122 as shown in Fig.3,

the number of the interconnect lines 122 extending from the inner interconnect pads 121 is restricted because the diameter of the interconnect pad 121 is generally larger than the width of the interconnect lines 122 and the interval of the adjacent lines.

When the interconnect pads 121 having a diameter of $100\mu\text{m}$ are arranged at a pitch of $250\mu\text{m}$, only two interconnect lines 122 can be drawn when the line width of the interconnect lines 122 is $30\mu\text{m}$ and the line interval is $30\mu\text{m}$. In other words, only 12 interconnect lines 122 can be arranged in an area having a width of 1 mm in the above structure of the interconnect pads 121, and the density of the interconnect lines is 12 lines/mm. When the number of the interconnect pads is increased to increase the number of the interconnect lines, the pitch of the interconnect pads is required to be larger than $250\mu\text{m}$ as described above or the chip size is required to be larger, thereby hardly realizing the miniaturization of the chip and the packaging substrate because the larger area is necessary to arrange the interconnect pads.

In order to solve such a problem, JP-A-10(1998)-116859 describes a technique in which interconnects pads for a standard power and a standard current which do not receive nor supply signals are disposed inside a package (chip) and the interconnects pads are connected to

external connecting terminals just below the chip. In the configuration, since the interconnect pad which does not receive nor supply signals is not required to be connected to the interconnect line, the interconnect line to be
5 arranged among the interconnect pads is unnecessary, thereby reducing the interval between the adjacent interconnect pads. As a result, the number of the interconnect pads can be increased and the miniaturization of the chip can be attained.

10 JP-A-9(1997)-69568 describes a technique in which an input-output buffer is disposed in an open region occurring in an inner circuit block-disposing area by not distinguishing an input-output buffer disposing area from the inner circuit block-disposing area in order to
15 realize the configuration which effectively utilizes the open area occurring in the inner circuit blocks without deteriorating the fundamental algorism of a tool for automatically disposing interconnects when the input-output buffer and the inner circuit block are disposed on
20 the chip. When the technique is applied on the chip or the package, at least the freedom of the disposition with respect to the disposition of the interconnect pads is elevated to effectively implement the miniaturization.

However, in the former publication, the number of
25 the interconnect pads which do not receive nor supply

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signals is assumed not to be small. Accordingly, the technique cannot be applied when the number of the interconnect pads of this kind is small and most part of interconnect pads are required to be connected to
5 interconnect lines. If the technique is applied to part of the interconnect pads, the number of the interconnect lines externally drawn is restricted.

In the latter publication, the number of the input-output buffers depends on the open area occurring among
10 the inner circuit blocks, and when the open areas are concentrated, it is uncertain that the interconnect lines are drawn from the input-output buffers. Accordingly, the interconnect pads must be designed for every floor plan to increase a period of time. When the drawing-out of the
15 interconnect lines is hardly attained, the effective means for responding thereto does not exist.

In the above technique, the interconnect line formed on the packaging substrate is assumed to be a single layer. When the interconnect line formed on the
20 packaging substrate is made to be a multi-layered structure having two or more layers, the structure increases the freedom of arranging the interconnect lines to assist to solve the above problem. However, the multi-layered structure may make the interconnect lines of the
25 upper layer and the lower layer crossed with each other

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to hardly perform the impedance matching among the interconnect lines, thereby affecting larger adverse effects on the semiconductor device.

5 SUMMARY OF THE INVENTION

In view of the foregoing, an object of the present invention is to provide a semiconductor device in which a chip or a package is miniaturized and the number of terminals of external connection terminals is increased.

10 Thus, the present invention provides a semiconductor device including: a semiconductor member having thereon a plurality of interconnect pads; and a mounting member having a plurality of electrode terminals electrically and mechanically connected to the
15 respective interconnect pads for mounting the semiconductor chip on the mounting member, the electrode terminals forming a plurality of I/O cells each having part of the electrode terminals, the part of electrode terminals including signal terminals, the I/O
20 cells forming a first group of the I/O cells and a second group of I/O cells disposed on an inner position of the mounting member with respect to the first group.

In accordance with the present invention, the higher integration of the semiconductor device having the
25 higher performances can be realized because the

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interconnect lines can be drawn to the outer periphery of the chip from the interconnect pads corresponding to each of the I/O cells when the chip is miniaturized or the number of the ball electrodes is increased.

5 Since the interconnect pads and the interconnect lines corresponding to the I/O cell is made by the single conductive film, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the
10 interconnect lines.

The above and other objects, features and advantages of the present invention will be more apparent from the following description.

15 BRIEF DESCRIPTION OF DRAWINGS

Fig.1 is a sectional view showing a conventional semiconductor device.

Fig.2 is a schematic view showing interconnect pads and interconnect lines arranged on a packaging substrate
20 of the conventional semiconductor device and an enlarged view showing a part of the arrangement.

Fig.3 is a schematic view showing the density of the conventional interconnect pads and interconnect lines.

Fig.4 is a vertical sectional view showing a
25 semiconductor device in accordance with a first

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embodiment of the present invention and an enlarged view thereof.

Fig.5 is a schematic view showing interconnect pads and interconnect lines arranged on a packaging substrate
5 of the first embodiment.

Fig.6 is a schematic view showing the density of the interconnect pads and the interconnect lines of Fig.5.

Fig.7 is a vertical sectional view showing a semiconductor device in accordance with a second
10 embodiment and an enlarged view thereof.

Fig.8 is a schematic view showing interconnect pads and interconnect lines arranged on a packaging substrate of the second embodiment.

Figs.9A to 9C are a schematic views showing first
15 modified examples of ball electrodes and the interconnect pads of the second embodiment.

Figs.10A to 10D are schematic views showing second modified examples of the ball electrodes and the interconnect pads of the second embodiment.

20 Figs.11A to 11 D are schematic views showing third modified examples of the ball electrodes and the interconnect pads of the second embodiment.

Figs.12A to 12D are schematic views showing fourth modified examples of the ball electrodes and the
25 interconnect pads of the second embodiment.

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Fig.13 is a flow chart sequentially showing steps for fabricating the semiconductor device of the present invention.

5 PREFERRED EMBODIMENTS OF THE INVENTION

Then, the configuration of a semiconductor device of a first embodiment will be described referring to Fig. 4.

10 A semiconductor device 11 includes a packaging substrate 12 and a chip 13 mounted thereon. The packaging substrate 12 is formed by a dielectric plate material and includes, on the top surface thereof, a plenty of interconnect pads 21 and interconnect lines 22 formed by etching a conductive film made of copper. The interconnect pads 21 and the interconnect lines 22 are
15 connected to for mounting ball electrodes 24 on the bottom surface of the packaging substrate 12 through intermediary of via-plugs 23 formed through the packaging substrate 12. A flame-like spacer 25 is fixed to the periphery of the top surface of the packaging
20 substrate 12 by using an adhesive agent, and accommodates the chip in the region surrounded the spacer 25. A covering plate 27 is fixed on the spacer 25 by using another adhesive agent 26 to seal the chip 13.

25 The chip 13 is formed by a semiconductor substrate such as silicon, and various elements such as a transistor

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not shown in the drawing are formed on the bottom main surface of the chip 13 and are covered with a protective dielectric film such as a passivation film. On the surface of the protective dielectric film or on the bottom surface of the chip are formed and arranged ball electrodes 31 made of solder, connected to the above elements, acting as internal electrodes. The ball electrodes 31 are soldered to the interconnect pads 21 formed on the packaging substrate 12 to mount the chip 13 on the packaging substrate 12 in a face-down manner, and the elements in the chip 13 are electrically connected to the ball electrodes 24 on the bottom surface of the packaging substrate 12 through intermediary of the ball electrodes 31 and the interconnect pads 21. The chip 13 is sealed is sealing resin 28.

In the first embodiment, the semiconductor device 11 is mounted on a mounting substrate 14. A specified interconnect pattern is formed on a dielectric substrate by using a conductive film to prepare the mounting substrate 14. The interconnect pattern includes interconnects pads 41 connected to the ball electrodes 24 of the semiconductor device 11 and interconnect lines, not shown in the drawings, for connecting the interconnect pads 41 among one another on the mounting substrate 14 or the interconnect pad 41 with interconnect lines not

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shown in the drawings for connecting the interconnect pad 41 to an external circuit.

An example of configuration will be described, referring to Fig.5, in which the ball electrodes 31 are formed and arranged on the bottom surface of the chip 13 of the semiconductor device 11 and interconnect pads 21 are formed and arranged on the top surface of the packaging substrate 12 corresponding to the ball electrodes 31.

10 The interconnect pads 21 formed on the top surface of the packaging substrate 12 shown in Fig.5 are disposed corresponding to the ball electrodes 31 on the bottom surface of the chip 13. The ball electrodes 31 on the bottom surface of the chip 13 are arranged in the shape of a lattice and the interconnect pads 21 are also arranged in the shape of the lattice corresponding to the ball electrodes 31. The specified number of the ball electrodes 31 and the interconnect pads 21 are grouped as a single I/O cell as shown in Fig.5 in which only the interconnect pads 21 are shown, and these are arranged as the I/O cell unit. In the embodiment, the plenty of the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The I/O cell is, for example, a single group including a single unit having one or more input-output buffers formed in the chip 13

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and an S-terminal (signal line terminal), a V-terminal (power source terminal) and a G-terminal (ground terminal) connected to the input-output buffers, or the single I/O cell may include only the S-terminal. However,
5 the number of the terminals and the arrangement are not restricted to the above, and an I/O cell having an arbitrary array can be formed.

Among the grouped I/O cells, part of the I/O cells (CELL-A) are disposed on the periphery of the chip 13
10 similarly to the conventional chip, and the remaining cells (CELL-B) are internally disposed from the above I/O cells (CELL-A) at a specified interval. In this case, the adjacent I/O cells (CELL-A) disposed on the periphery have a specified space therebetween. In the first
15 embodiment, if the additional space exists between the adjacent I/O cells (CELL-A), peripherals (PL) conventionally used are also disposed on the chip. The peripherals are present in the open space in the 4 x 3 array.

20 As shown in Fig.6, two outer peripheral I/O cells (CELL-A) on the chip 13 are disposed with a specified interval along the periphery, and one inner I/O cell (CELL-B) is disposed in a space opposing to the location between the two outer peripheral I/O cells (CELL-A).
25 Similarly to the preceding example, the interconnect lines

22a are connected to each of the interconnect pads 21a of the two outer peripheral I/O cells (CELL-A), and are drawn between the interconnect pads 21a to regions external to the chip 13. On the other hand, the
5 interconnect lines 22b are connected to each of the interconnect pads 21b of the inner peripheral I/O cell (CELL-B), and are drawn similarly to the preceding example in the region of the peripheral I/O cell (CELL-B), and are bundled at a specified interval, at a region out of
10 the inner peripheral I/O cell (CELL-B), to be drawn between the outer peripheral I/O cells (CELL-A) to regions external to the chip 13.

In the structure of the interconnect pads 21 and the interconnect lines 22 on the packaging substrate 12, the
15 density of arranging the interconnect lines 21a at the I/O cells (CELL-A) arranged on the outer periphery of the chip 13 is substantially same as the density of the conventional device shown in Fig.3. However, the density of arranging the interconnect lines 21b connected to the
20 interconnect pad 21b of the I/O cells (CELL-B) arranged inside of the chip 13 can be increased because of the absence of the interconnect pads.

When the line width of the interconnect lines connected to the 12 interconnect pads 21 is $30\mu\text{m}$ and
25 the line interval is $30\mu\text{m}$ as shown in Fig.6, the

dimension of arranging the 12 bundled interconnect lines 22i is $750\mu\text{m}$. The number of the interconnect lines 22 in the region having a size of 2 mm along the outer periphery of the chip is 27 calculated by adding the
5 number of the interconnect lines 22a of the outer peripheral I/O cells (CELL-A) to the number of the interconnect lines 22b of the inner I/O cells (CELL-B). The density of the interconnect lines 22 is 13.5 lines/mm in the embodiment, and is increased compared with
10 conventional density of 12 lines/mm shown in Fig.3.

Thereby, even when the size of the chip 13 is reduced for miniaturization or the numbers of the ball electrodes 31 and the interconnect pads 21 are increased with the chip 13 having the same size, the higher
15 integration of the semiconductor device having the higher performances can be realized by dividing the ball electrodes 31 disposed on the chip 13 and the interconnect pads arranged on the packaging substrate 12 into the plurality of the I/O cells and disposing part of
20 the I/O cells at the outer periphery of the chip 13 and the remaining I/O cells at the corresponding inner sections of the chip 13 because the drawing-out of the interconnect lines 22 to the peripheral outer regions of the chip on the top surface of the packaging substrate 12 is possible.

25 Especially, as shown in Fig.6, since the interconnect

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lines of the other I/O cells do not pass through the I/O cells (CELL-B) disposed on the inner section of the chip, the I/O cells (CELL-B) may be formed endlessly or annually to enable the arrangement of the extremely
5 larger number of the ball electrodes 31 and the interconnect pads 21. An interval may exist between the I/O cells (CELL-B) disposed on the inner section. The ball electrodes 31 and the interconnect pads 21 of the outer peripheral I/O cells (CELL-A) may be freely disposed so
10 long as the spaces through which the interconnect lines 22 of the I/O cells (CELL-B) disposed on the inner section pass may be secured, thereby promoting the higher integration of the semiconductor device having the higher performances. The I/O cells can be freely disposed in the
15 regions of the chip so long as the above requisites are satisfied to increase the freedom of the chip design and the package design.

Since the interconnect pads 21 and the interconnect lines 22 in the embodiment are made by the
20 conductive film having the single layer, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines. Especially, when the interconnect pads and the interconnect lines
25 corresponding to the plurality of the input-output buffers

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are intermingled in the single I/O cell, the proper impedance matching is possible by preventing the mutual intervention between the interconnect lines of each of the input-output buffers.

5 A second embodiment of the present invention is shown in Fig.7 in which the same numerals as those of the first embodiment designate the same elements. A semiconductor device 11 includes a packaging substrate 12A and a chip 13 mounted thereon. The packaging
10 substrate 12A includes a central core layer 211 sandwiched between a pair of buildup layers 212, 213, and a plenty of interconnect pads 21 made of a conductive film are formed on the top buildup layer 212. The interconnect pads 21 are connected to the interconnect
15 lines in each of the multi-layers of the top buildup layer 212, further connected to the bottom buildup layer 213 through intermediary of via plugs, and still further connected to ball electrodes 24 formed on the bottom surface of the bottom buildup layer 213 or the bottom
20 surface of the packaging substrate 12A.

Each of the buildup layers is multi-layered, and the top buildup layer 212 includes five interconnect layers in which a first layer includes the interconnect pads 21 and a GND layer, a third layer includes a GND layer 3G and a
25 VDD layer 3V, and a fifth layer includes a GND layer 5G

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and a VDD layer 5V connected to the via plugs of the above core layer. A second layer and a fourth layer are formed as independent interconnect lines 22a, 22b for signals. In the second embodiment, the interconnect lines
5 formed in the single layer in the first embodiment are divided into the first to fifth interconnect layers 201 to 205. Especially, the interconnect lines connected to the interconnect pad 21 acting as the S-terminal (signal terminal) can be drawn as the interconnect lines 22 of the
10 second and fourth layers separately from the others.

In view of the increased number of layers (two-layered) of the interconnect lines 22a, 22b, as schematically shown in Fig.8, the grouped I/O cell in the arrangement of the interconnect pads 21 as well as the
15 ball electrodes 31 of the chip 13 can be divided into a first I/O cell (CELL-1) and a second I/O cell (CELL-2). Part of the first I/O cell (CELL-1) or I/O cells (CELL-1A) are disposed on the outer peripheral region of the chip 13, and the remaining I/O cells (CELL-1B) are disposed on
20 the inner sections of the chip 13. Intervals are secured between the first I/O cells (CELL-1A) remaining on the outer periphery for passing the interconnect lines 22 drawn from the inner I/O cells (CELL-1B). In Fig.8, the first I/O cells (CELL-1) disposed on the outer periphery
25 are alternately disposed on outer sections (CELL-1A) and

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inner parts (CELL-1B) in the outer periphery. The second I/O cells (CELL-2) are disposed on the sections inside of the other I/O cells (CELL-1), and part of the second I/O cell (CELL-2) or I/O cells (CELL-2B) are disposed inside
5 of the remaining I/O cells (CELL-2A) and intervals are secured between the outer second I/O cells (CELL-2A) for passing the interconnect lines drawn from the inner second I/O cells (CELL-2B). In Fig.8, similarly to the first I/O cells (CELL-1), the second I/O cells (CELL-2) are
10 alternately disposed on outer sections (CELL-2A) and inner parts (CELL-2B).

Referring again to Fig.7, the interconnect line 22-1 connected to the interconnect pad 21-1 of the first I/O cell (CELL-1) is connected in its outer region to the second
15 interconnect layer 202 of the top buildup layer 212 and drawn to the outer region by the second interconnect layer 202. The interconnect line 22-2 connected to the interconnect pad 21-2 of the second I/O cell (CELL-2) is connected in the area between its outer region and the
20 first I/O cell (CELL-1) to the fourth interconnect layer 204 of the top buildup layer 212 and drawn to the outer region by the fourth interconnect layer 204. Accordingly, the interconnect line 22-2 connected to the second I/O cell (CELL-2) is never drawn to the outer region through the
25 first I/O cells (CELL-1). The interconnect lines 202, 204 of

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the second and the fourth layers are connected to the via plugs 23 of the core layer 211 at specified positions and further connected to the ball electrodes 24 on the bottom surface of the packaging substrate 12A through
5 intermediary of the bottom buildup layer 213.

The configuration of the interconnect pads 21 and the interconnect lines 22 on the top surface of the packaging substrate 12A obtained in this manner is similar to that shown in Fig.6 for each of the first I/O cell
10 (CELL-1) and the second I/O cell (CELL-2), and enables to elevate the density of the interconnect pads 21 and the interconnect lines 22 of the first I/O cell (CELL-1) and the second I/O cell (CELL-2). Since the first I/O cell (CELL-1) and the second I/O cell (CELL-2) are double-disposed in
15 the second embodiment, the density almost twice that of the first embodiment can be obtained. Thereby, even when the chip is miniaturized or the numbers of the ball electrodes and the interconnect pads are increased, the higher integration of the semiconductor device having the
20 higher performances can be realized by drawing the interconnect lines of each of the I/O cells.

Since the interconnect lines 22-1 of the first I/O cell (CELL-1) is drawn by the second interconnect layer 202 and the interconnect lines 22-2 of the second I/O cell
25 (CELL-2) is drawn by the fourth interconnect layer 204 in

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the second embodiment, the interconnect lines connected to the respective I/O cells are drawn to the single interconnect layer and are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines. Especially, when the interconnect pads and the interconnect lines corresponding to the plurality of the input-output buffers are intermingled in the single I/O cell, the proper impedance matching is possible by preventing the mutual intervention between the interconnect lines of each of the input-output buffers similarly to the first embodiment.

Modified first examples of arranging the first I/O cell (CELL-1) and the second I/O cell (CELL-2) in the second embodiment are shown in Figs.9A to 9C. In Fig.9A, only for the first I/O cell (CELL-1), the outer I/O cell (CELL-1A) and the inner I/O cell (CELL-1B) are disposed. In Fig.9B, only for the second I/O cell (CELL-2), the outer I/O cell (CELL-2A) and the inner I/O cell (CELL-2B) are disposed. As shown in Fig.9C, each of the first I/O cell (CELL-1) and the second I/O cell (CELL-2) may be disposed in a single row.

Modified second examples of arranging the I/O cells in the second embodiment are shown in Figs.10 A to 10D in which either of the first I/O cell (CELL-1) and the second I/O cell (CELL-2) is not the I/O cell but the

conventional peripherals. In Fig.10A, the outer peripheral section is formed by peripherals PL and the inner section is formed by the second I/O cell (CELL-2). In Fig.10B, the inner second I/O cell (CELL-2) of Fig.10A is
5 formed by the outer I/O cell (CELL-2A) and the inner I/O cell (CELL-2B). In Fig.10C, the outer peripheral section is formed by the first I/O cell (CELL-1) and the inner section is formed by the peripherals PL. In Fig.10D, the outer first I/O cell (CELL-1) of Fig.10C is formed by the
10 outer I/O cell (CELL-1A) and the inner I/O cell (CELL-1B).

As shown in Figs.11A to 11D corresponding to Figs.10A to 10D, respectively, part of the first I/O cell (CELL-1) or the second I/O cell (CELL-2) is formed by the
15 peripherals PL to intermingle the I/O cells and the peripherals PL. Similarly, as shown in Figs.12A to 12D, part of the first I/O cells (CELL-1A, CELL-1B) or the second I/O cells (CELL-2A, CELL-2B) formed by the inner I/O cells and the outer I/O cells may be formed by
20 the peripherals PL. In either case, the higher integration of the semiconductor device having the higher performances can be realized compared with the conventional configuration as shown in Fig.2 because the ball electrodes and the number of the interconnect pads
25 can be increased.

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The method of disposing the ball electrodes 31 and the interconnect pads 21 as the I/O cells are substantially same for the semiconductor devices of the first and the second embodiments. The method for disposing the semiconductor device in the first embodiment will be
5 described referring to a flow chart shown in Fig.13.

At first, a template having I/O cells and peripherals to be disposed on a chip along the outer periphery of the chip is fabricated (S101). Then, the judgment is
10 conducted whether or not the numbers of the balls electrodes and the interconnect pads of the I/O cell and the peripherals, and the number of required terminals reach to specified values (S102). When the numbers reach to the required values, the judgment is conducted
15 whether or not the request for disposing I/O cells at the center of the chip (S103). In absence of the request, the disposal is finished (S104). In present of the request for disposing the I/O cells at the center of the chip, the cell is moved in accordance with a floor plan (S105). When the
20 movement is possible, the disposal is finished (S104). When the movement is impossible, the step (S105) is again executed after the floor plan and the I/O cells are modified. When the movement is also impossible after the repetition of the processes, a following step (S108) is
25 initiated.

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On the other hand, when the number of the terminals does not reach to the required number in the step (S102), the number of the I/O cells disposed on the inner sections of the chip is calculated (S107) for increasing the number to the required one. Then, another new template having a reduced interval between the I/O cells is fabricated (S108). Then, the I/O cell is moved in accordance with a floor plan (S109). When the movement of all the I/O cells is possible, the disposal is finished (S104) because the I/O cells can be disposed on the outer periphery and on the inner section of the chip. When at least one of the I/O cells cannot move, the step (S109) is again executed after a further template having a reduced interval between the I/O cells is fabricated (S110). Or, depending on necessity, the step (S109) is again executed after the modification of the floor plan and the I/O cells. When the disposal of all the I/O cells is not finished after the plurality of the re-executions, the disposal is recognized to be failed, and the procedures are started from the first step (S101) after the chip is enlarged or the number of the interconnects is increased.

In the second embodiment, a process of diving the I/O cell into the first I/O cell and the second I/O cell is inserted between the steps (S107) and (S108), and the processes are conducted on and after the step (S108) for

each of the I/O cells.

In the method described above, after the I/O cell is formed by grouping the S-terminal, the V-terminal and the G-terminal, the method of disposing the interconnect pads of the I/O cell and drawing the interconnect lines
5 connected to the interconnect pads is determined in advance. Thereby, the propriety of drawing the interconnect lines at the time of preparing the floor plan can be easily judged to advantageously reduce a length of
10 processing time (TAT). The method can be easily customized for every kind of the semiconductor devices by suitably using the I/O cells having different usages after the usages of each of the I/O cells are stored as information.

15 Although the array of 4 x 3 is exemplified as the arrangement of the I/O cells in the previous embodiments, the I/O cells can be arranged in an array having an arbitrary number. Depending on cases, the I/O cell may be formed by disposing the plurality of the conventional
20 peripherals.

Although the examples are described for applying the configuration of the present invention to the ball electrodes 31 formed on the bottom surface of the chip 13 and the interconnect pads 21 and the interconnect lines
25 22 on the packaging substrate 12, 12A in the preceding

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embodiments, the present invention may be also applied to the ball electrodes 24 of the semiconductor device 11 and the interconnect pads 41 and the interconnect lines on the mounting substrate 14. The ball electrodes 24 on the bottom surface of the packaging substrate 12, 12A and the interconnect pads 41 on the top surface of the mounting substrate 14 are disposed as the I/O cells to increase the density of the ball electrodes 24 and the interconnect pads 41 to achieve the miniaturization of the chip and further to increase the number of the terminals, the higher integration of the semiconductor device having the higher performances can be realized. When the configuration of the second embodiment is applied, the mounting substrate 14 is multi-layered.

Since the above embodiment is described only for examples, the present invention is not limited to the above embodiment and various modifications or alterations can be easily made therefrom by those skilled in the art without departing from the scope of the present invention.

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